



# PCIe® CEM 4.0 Previews

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# Disclaimer



The information in this presentation refers to specifications still in the development process. This presentation reflects the current thinking of various PCI-SIG® workgroups, but all material is subject to change before the specifications are released.

# Agenda



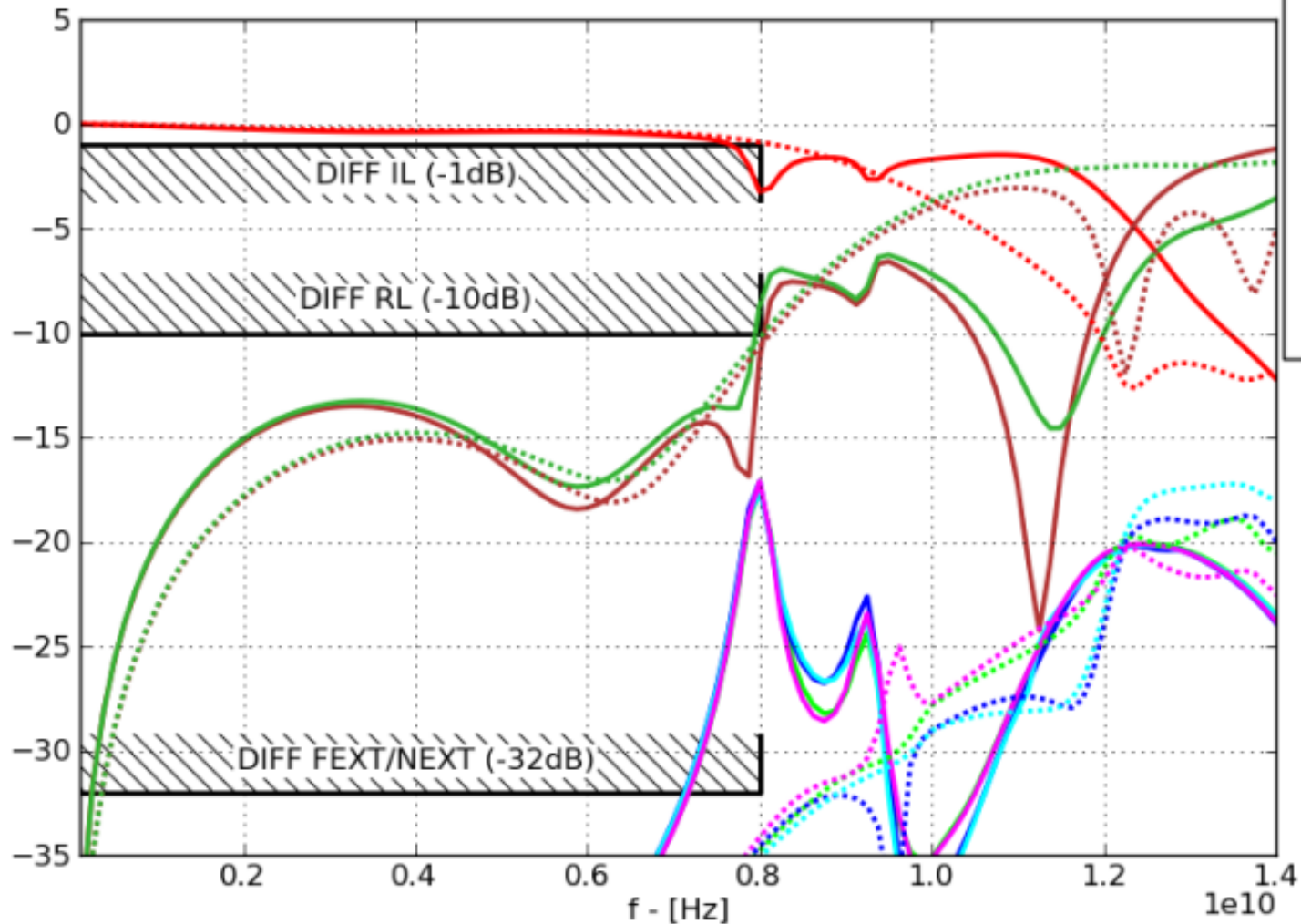
- **PCIe® 4.0 CEM Goals**
- **PCIe 4.0 CEM Connector Direction**
- **PCIe 4.0 Tx Limits and Test Fixtures**
- **Summary and Conclusions**

# PCI Express® 4.0 CEM Goals



- **Full backwards interoperability with PCIe 1.x, PCIe 2.x, PCIe 3.x**
- **Same channel reach as for PCIe 3.0 with improvements**
  - Client: 10-14 inch, one connector
  - Server: 20 inch, two connectors – requires a Retimer
- **Minimize required changes to the connectors, card form factors, or material**
- **Minimal changes to the measurement methodologies from those used in the PCIe 3.x specifications**
  - Use eye diagrams (jitter/voltage margin requirements). Minimize additional new requirements.

# Minimum 4.0 Target Connector Performance



**High Degree of Confidence That Backwards Compatible Solutions Possible**

# 4.0 Connector/Card Goals



- **Mitigate conductor geometry that impairs performance in the PCIe connector at 16GT/s**
- **Preserve full backwards compatibility among combinations of 2.5-5-8-16 GT/s connectors and Add-in Cards (AIC)**
- **Keep the standard thru-hole pinfield, for thru-hole parts (if possible)**
- **Define a common surface mount connector footprint and related specifications**
- **Build test boards and characterize and correlate models for the proposed performance enablers**

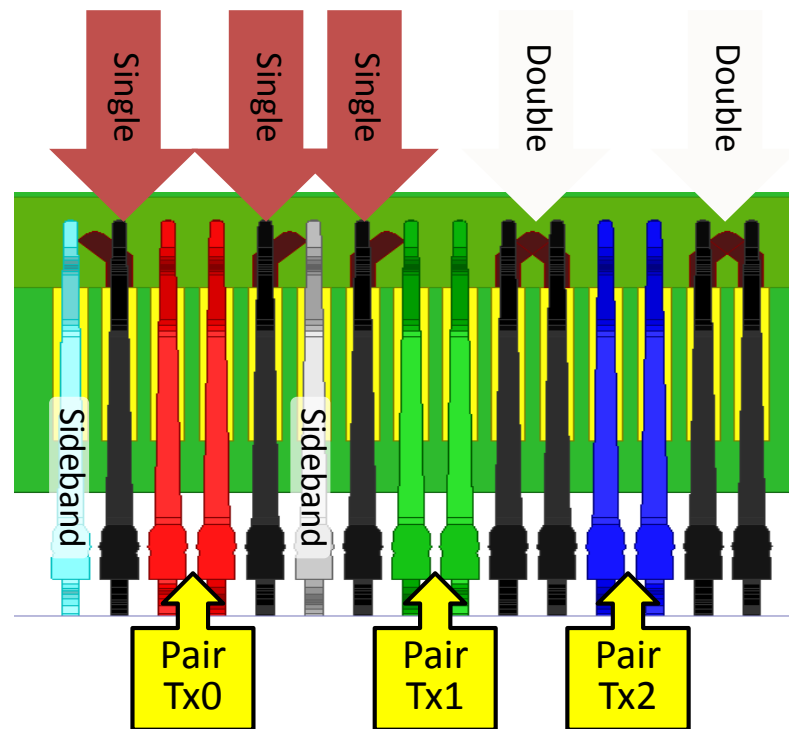
# Connector Enabler Conclusion



- **These enablers indicate that a thru-hole solution is feasible with the same motherboard pinout as 3.0**
- **CEM 4.0 references both approaches (improvements to work with existing thru-hole pinout vs SMT connectors)**
- **Current plan for 4.0 CEM is to support and specify both thru-hole and SMT connectors for 4.0**
- **Built test boards to obtain lab data for each potential enabler with both through-hole (PTH) and surface mount (SMT) connectors**

# Signal & Ground Pin Assignment

- **The pin assignments in the connector are non-uniform**
  - Note that the quantity of ground pins (Black) adjacent to the diff pairs are “Single” or “Double”
  - The electrical behavior of pairs having “Single” or “Double” grounds differs
  - Test board experiments target single or double ground, or a combination





# PCIe 4.0 Experiments



## On the Add-in Card PCB:

1. **Baseline Typical 8GT/s**
2. **Adjacent ground vias (required)**
3. **Join the ground edge fingers**
4. **Narrow the ground fingers**
  - Improves overall insertion loss
  - Ground finger resistive termination
5. **Ground finger resistive termination**
  - Suppresses all resonance
6. **Place floating subsurface resonant structures beneath ground fingers**
  - Suppresses resonant insertion loss/crosstalk spikes
7. **Multi enabler experiments**

## Baseboard & Connector changes:

1. **Surface mount connector**
2. **Thru Hole with stub**
3. **Thru Hole with no stub**
4. **Thru Hole with via stub mitigation**
  - Reduces baseboard PCB via resonance

# Test Layout 1: Baseline

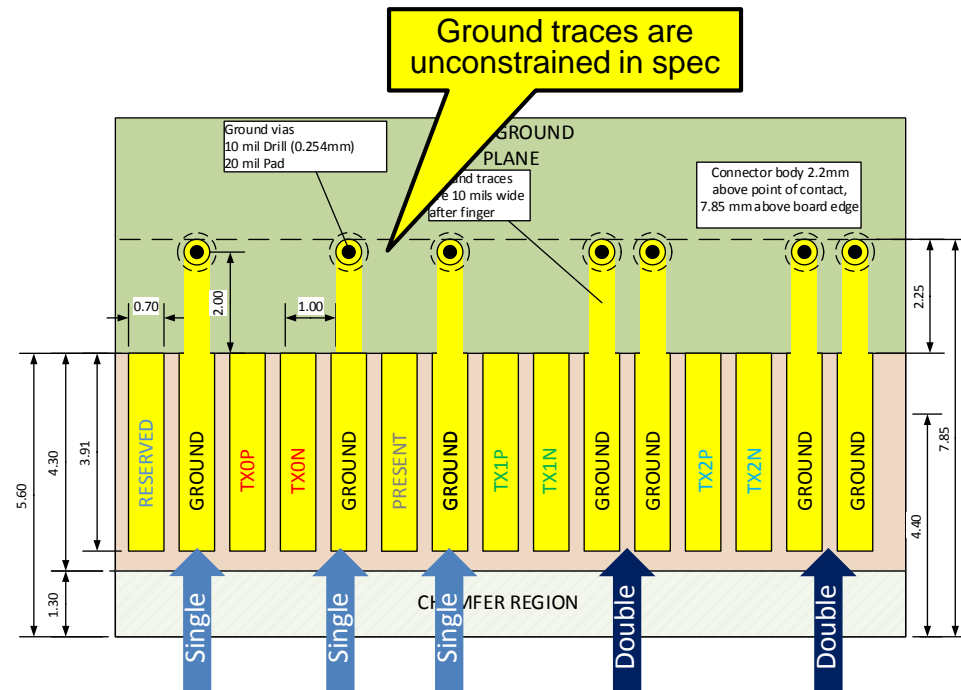
- The trace between the via and ground finger is not addressed in the CEM spec

- The length, width, and shape of the ground trace has been implementation specific

- The ground traces, above the ground finger, may be straight, like here ↗ or hockey-stick, etc.

- For this baseline test, use these common PCIe 3.0 edge finger dimensions

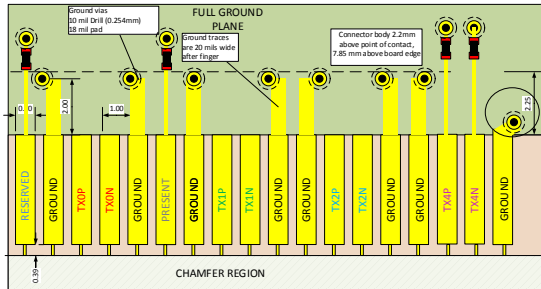
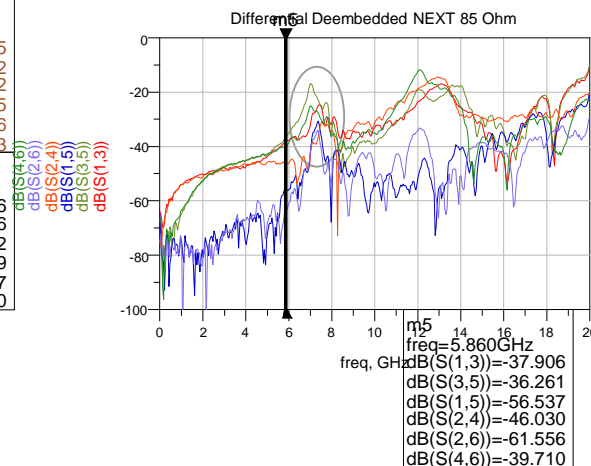
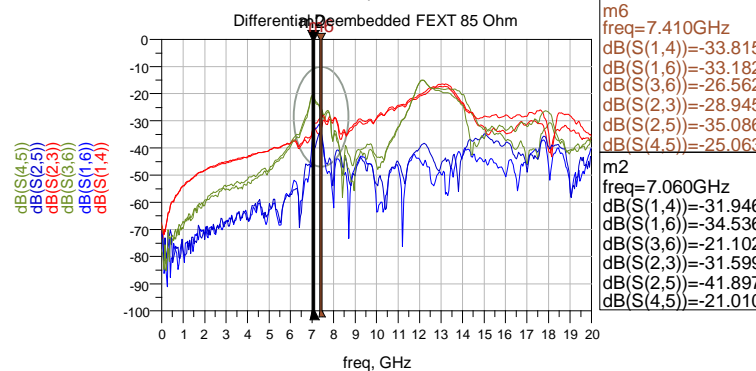
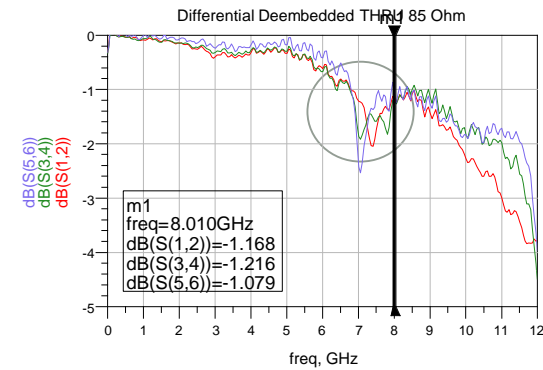
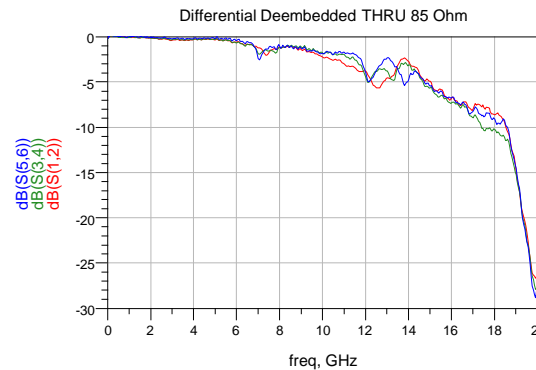
- 2mm long, 0.508mm (20 mil) wide ground trace, as shown



# Baseboard – Thru-hole, No Via Stub

- AIC Baseline cluster. No improvements to card.

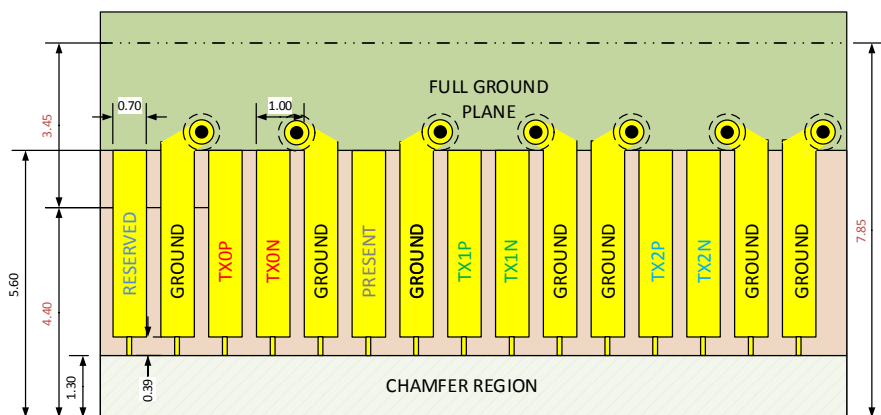
- FEXT/NEXT spike near 7-8GHz



# Test Layout 2: Adjacent Ground Vias

## Test 2a One via per finger

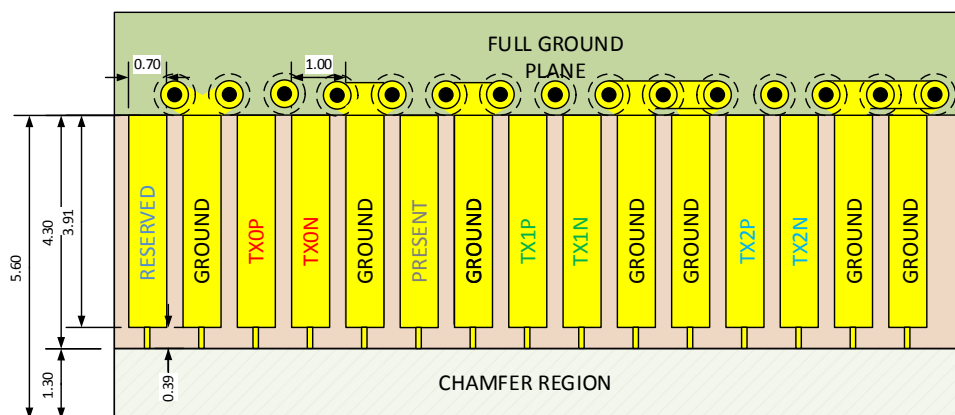
- Fewest drills
- Not joining adjacent grounds
- Vias must fall between fingers to permit the escape of signals on the back side
- Most vias are reused by the ground fingers on the reverse side of the PCB



## Test 2b Two vias per finger

- More drills, risk of mechanical weakening
- Adjacent grounds are joined
- Additional vias for backside doubles shown

1mm pitch with 10 mil drills  
results in 25% reduction in  
PCB "web" width (vs. no vias)

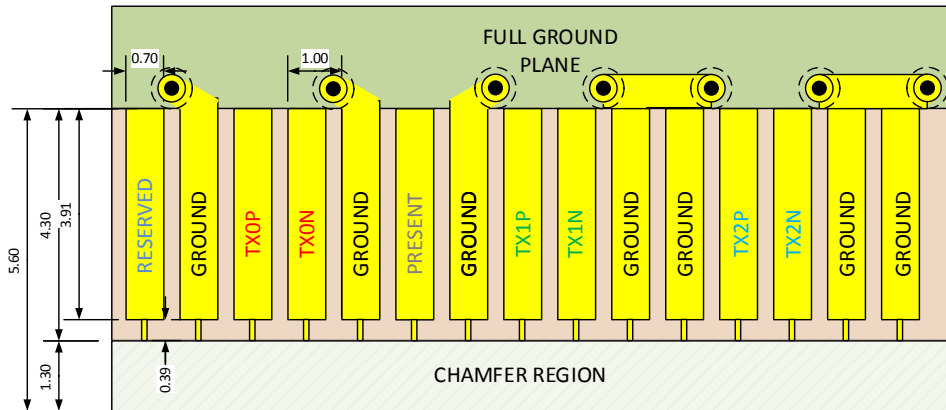


# Test Layout 2: Adjacent Ground Vias

## ○ Test 2c One via per finger

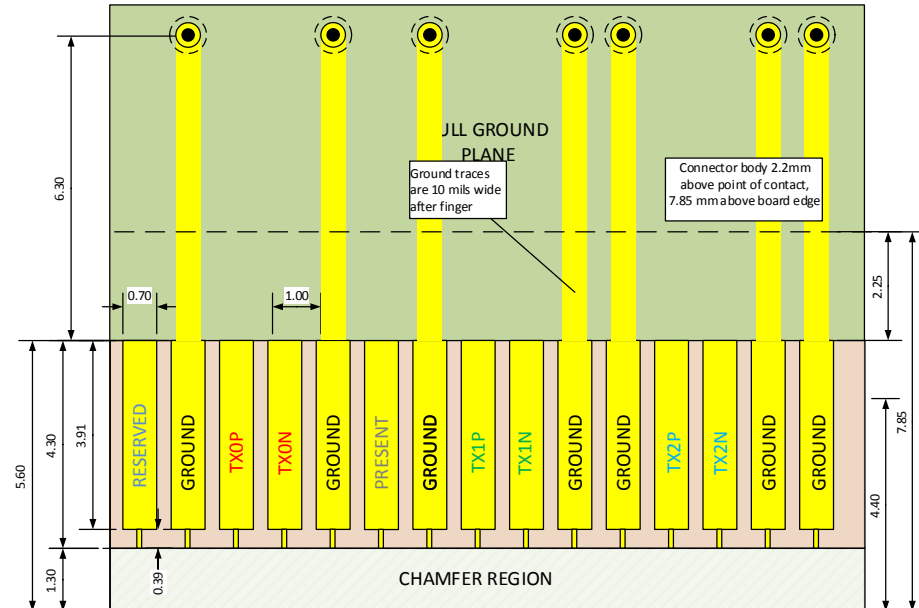
- Fewest drills
- Join Adjacent Grounds
  - But no middle drill

Note, most vias are reused by the Rx side grounds on the reverse side of the PCB



## ○ Test 2d Very long ground connection

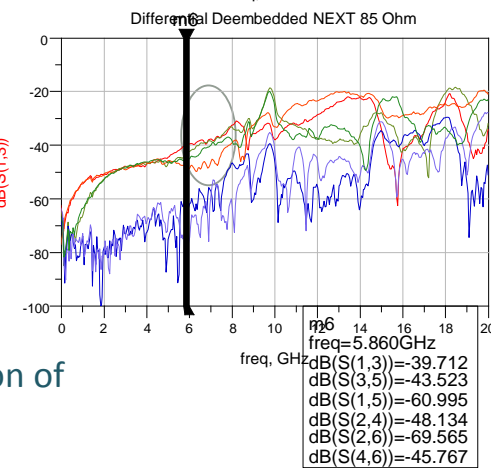
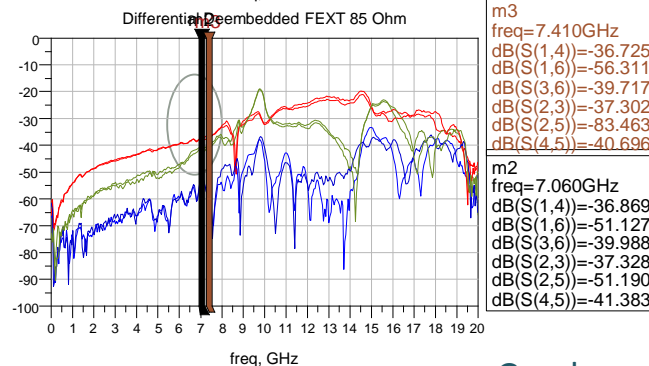
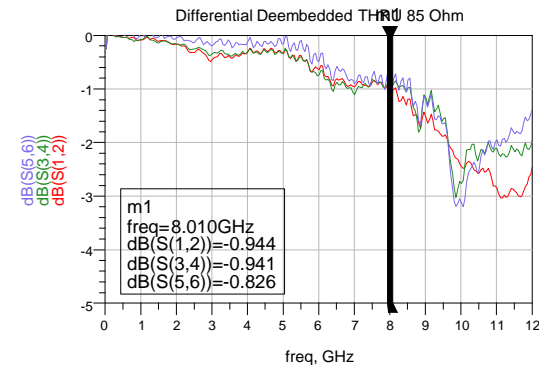
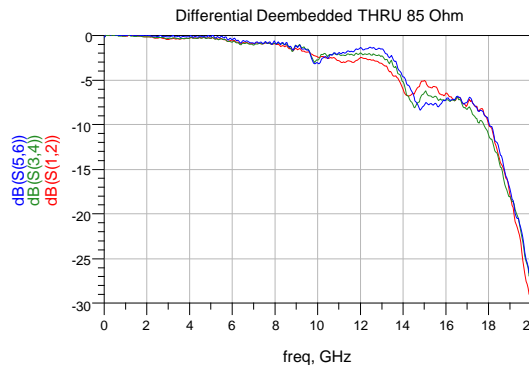
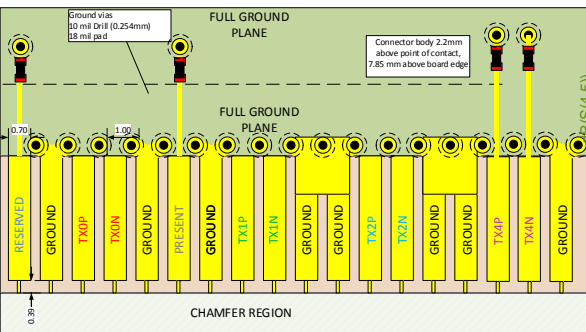
- Worst case 6.3mm, taken from real-world layout



# Baseboard – Thru-hole, No Via Stub

## Improved AIC Test

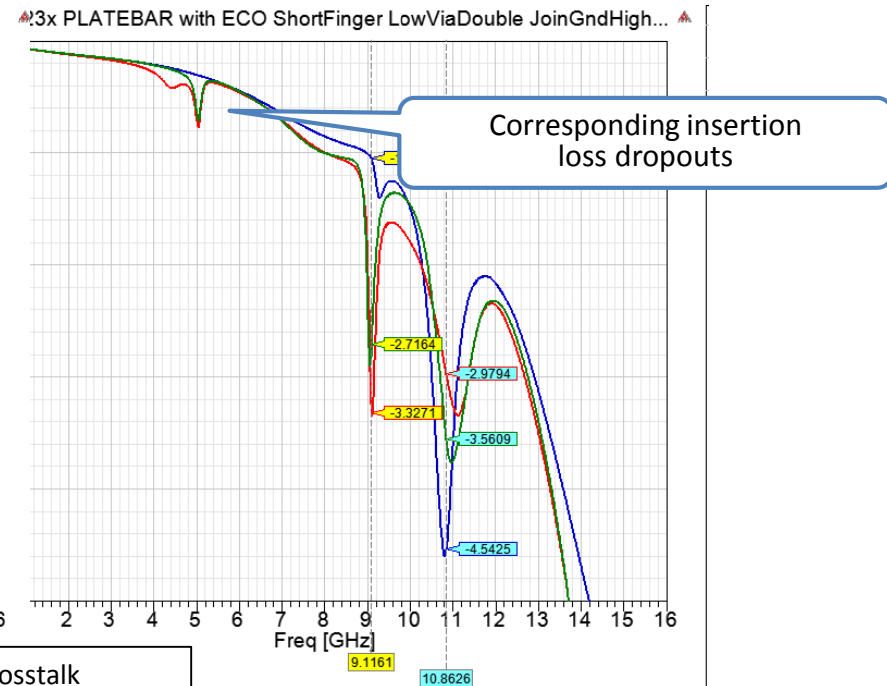
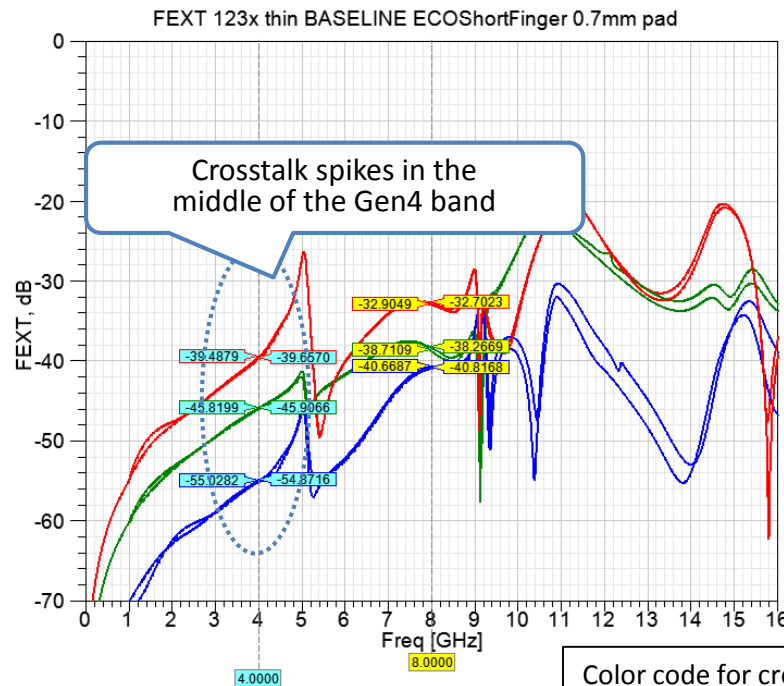
- Lower ground
- Joined double Gnd



Good suppression of  
FEXT/NEXT

# Sideband Signal Termination

- If the floating conductors are terminated with an open circuit, they can resonate, as they couple energy in/out of their neighbors
  - Multiple reflections will manifest as a spike at the resonant frequency
  - Similar results with a short circuit



Color code for crosstalk

Lane 0 ↔ Lane 1

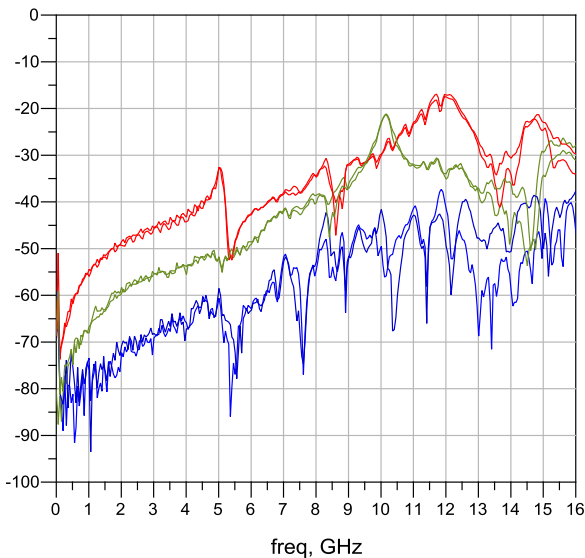
Lane 1 ↔ Lane 2

Lane 0 ↔ Lane 2

# Cross-talk w/wo Termination

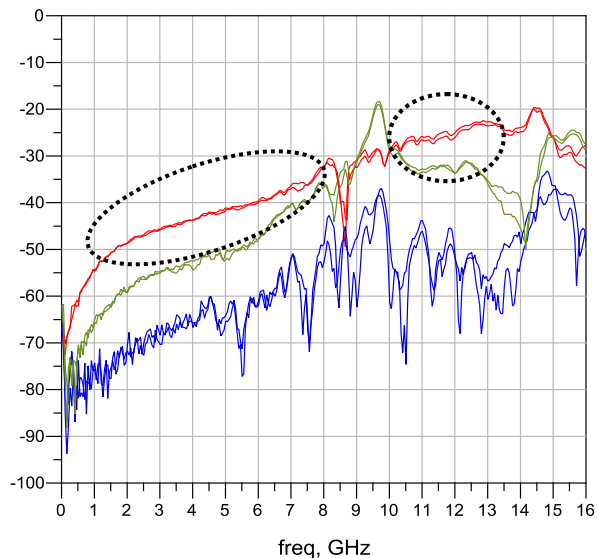
No termination resistors

Measured Differential Deembedded FEXT 85 Ohm



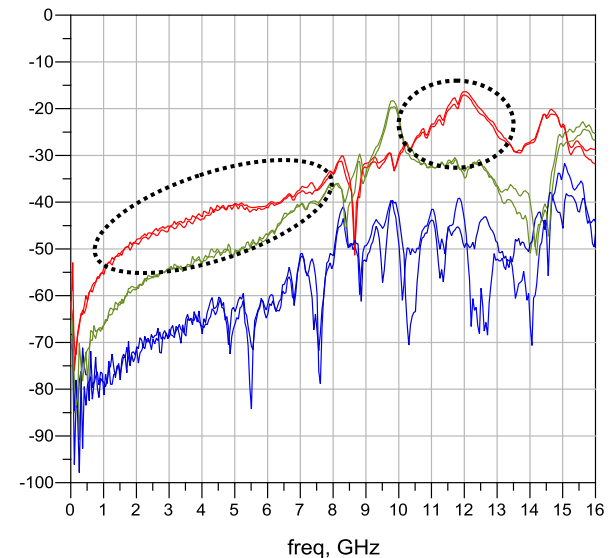
Resistors on both ends

Measured Differential Deembedded FEXT 85 Ohm



Resistors on one end  
(add in card only)

Measured Differential Deembedded FEXT 85 Ohm



Color code for crosstalk

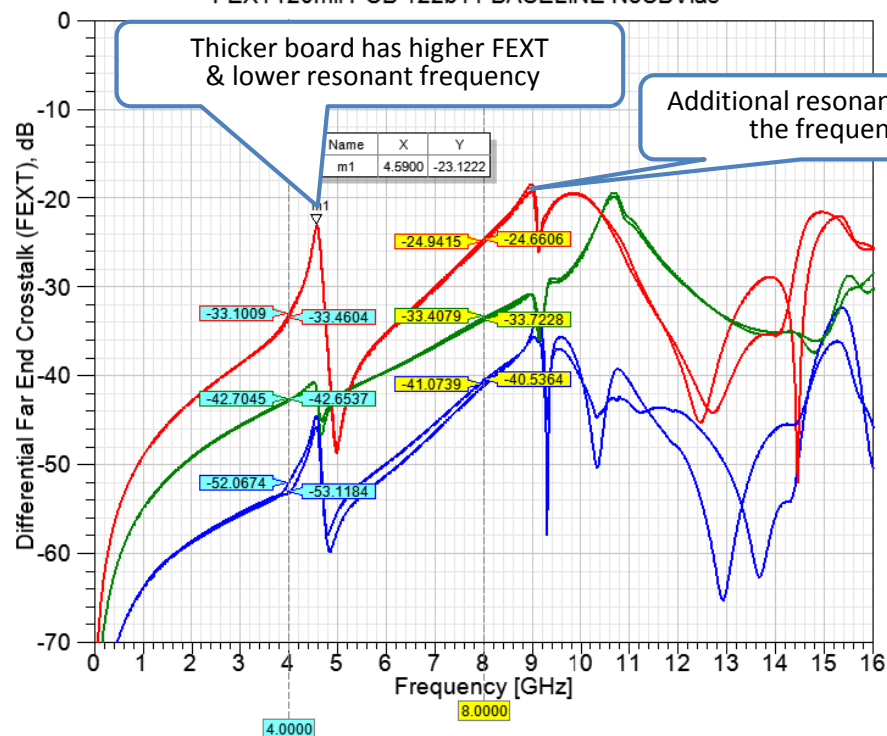
Lane 0 ↔ Lane 1   Lane 1 ↔ Lane 2   Lane 0 ↔ Lane 2



# Compare 120 mil vs. 62 mil Baseboard

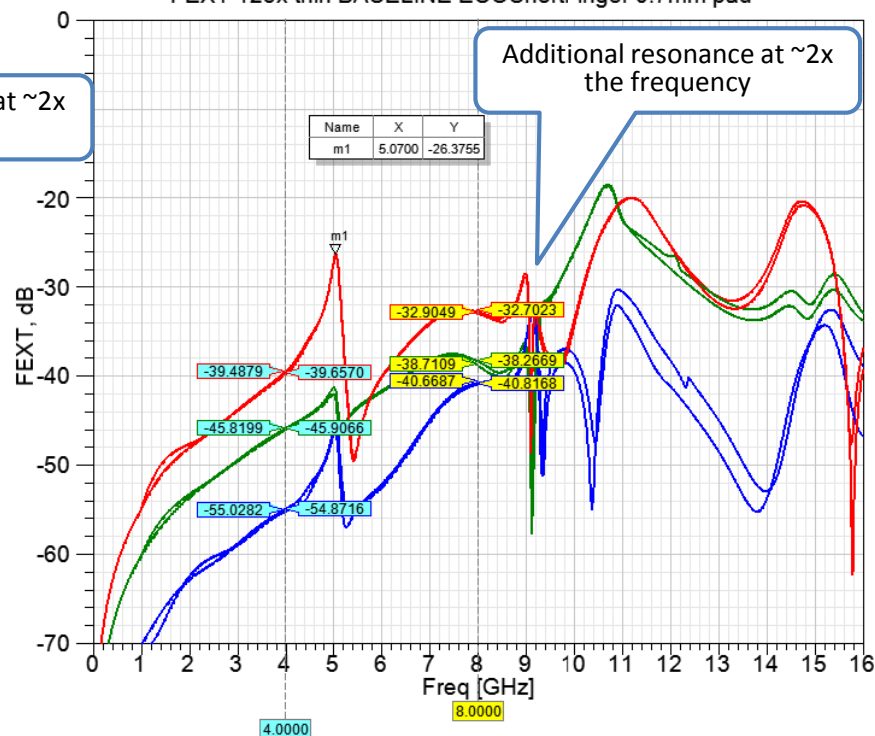
120 mil baseboard

FEXT120mil PCB 122b11 BASELINE NoSBVias

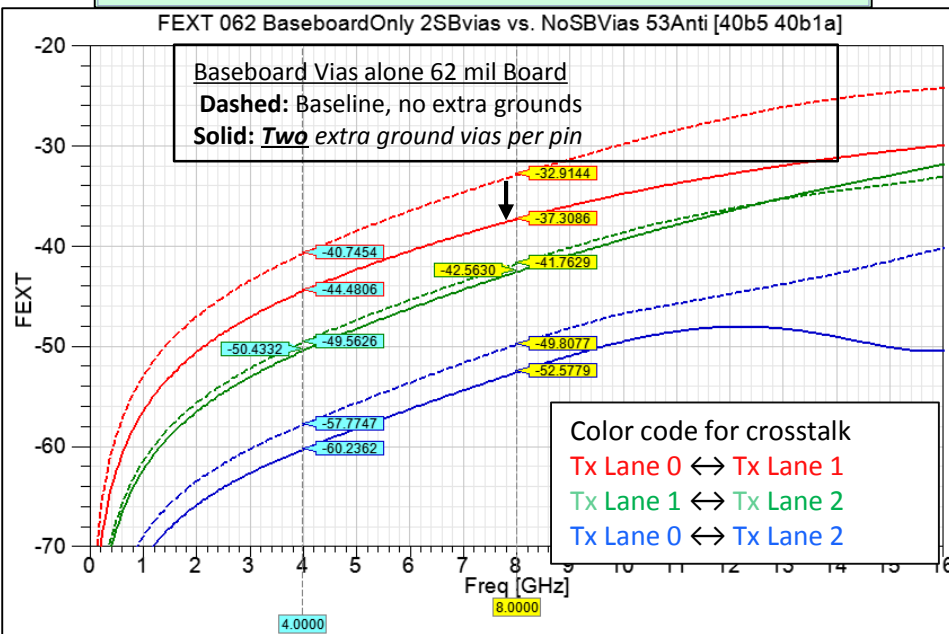
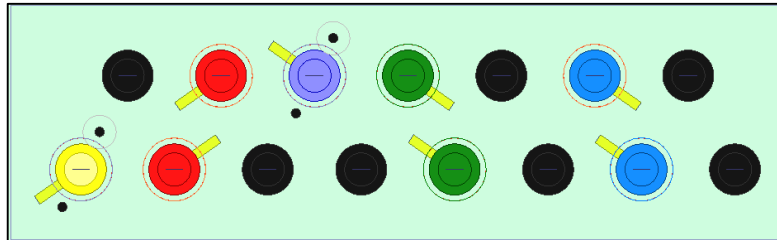


062 mil baseboard

FEXT 123x thin BASELINE ECOShortFinger 0.7mm pad



# Add 2 Baseboard Ground Sentry Vias



## ○ Adding two vias per sideband pin improves the worst case FEXT

- Lane 0 ↔ Lane 1 FEXT drops by about 4.5dB across much of the 0-8 GHz band
- Lane 1 ↔ Lane 2 largely unaffected  
Lane 0 ↔ Lane 2 are

# Simulation Results Example

## ○ All Enablers Except Sentry Vias

Lane 0	Lane 1	Lane 2		Lane 0	Lane 1	Lane 2
9.58	19.15	23.39	← No Termination →	14.40	19.15	22.55
17.36	21.75	23.28	← Terminate Board end 1pF →	18.65	21.65	22.45
16.30	21.99	22.75	← Terminate Card end 1pF →	19.35	21.80	21.85
19.55	22.28	23.50	← Terminate Both ends 1pF →	20.25	22.05	22.65
19.28	22.22	23.54	← Terminate Both ends 10pF →	20.00	22.05	22.65
30.14	30.52	30.12		25.15	25.65	25.10

## ○ With Sentry Vias (4 per Sideband)

Eye Height (higher is better)			Sentry vias & other enablers	Eye Width (higher is better)		
Lane 0	Lane 1	Lane 2	Termination variation	Lane 0	Lane 1	Lane 2
30.14	30.52	30.12	← No Connector →	25.15	25.65	25.10
23.27	24.93	24.36	← No Termination →	22.55	23.35	22.95
23.27	24.93	24.36	← Terminate Board End →	22.55	23.35	22.95
24.65	24.86	25.12	← Terminate Card End →	23.20	23.05	23.25
25.33	25.51	25.14	← Terminate Both Ends →	23.95	24.25	23.15

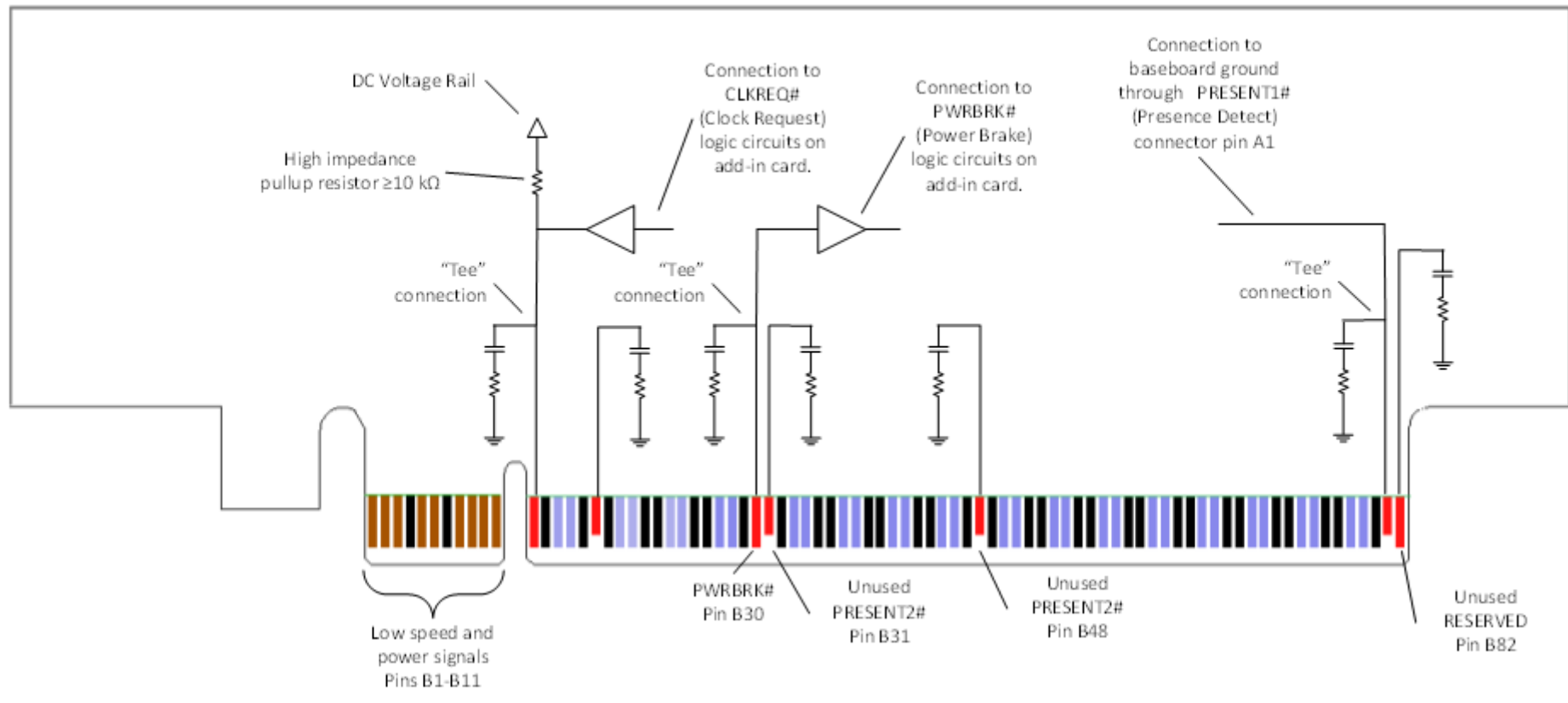
# Required Connector Enabler Summary



- **Adjacent Add-in Card Ground Vias (15 mil maximum distance)**
  - Joined double grounds
- **Sentry Vias in the Base Board Pinfield (min 2)**
- **AC Sideband Termination on Add-in Cards**

***Minor PCB Changes Enable 3.0 Through-Hole CEM Connector to Work for 4.0***

# AC Sideband Termination



**AC Sideband Termination 4.0 CEM Specification Targets are 43 ohm and 1 pf**

# PCIe 4.0 CEM Connector Test Results



- **Testing results over several vendors and parts with standalone 4.0 test fixtures produced mixed results**
  - Several vendors/parts 3.0/4.0 PTH connectors look great with improvements
    - IL < 1.5 dB to 8 GHz
    - RL < 10 dB to 8 GHz
    - Cross-talk < 40 dB to 8 GHz
  - Several vendors/parts show IL/cross-talk spikes around 8 GHz
    - IL spikes to ~ 3 dB
    - Cross-talk spikes to ~20 dB
    - Link impact for these cases may not be significant <1" – but requires careful analysis

**Multiple vendors/parts meet 4.0 CEM targets with improvements**

# PCI Express 3.0/4.0 Channel Analysis



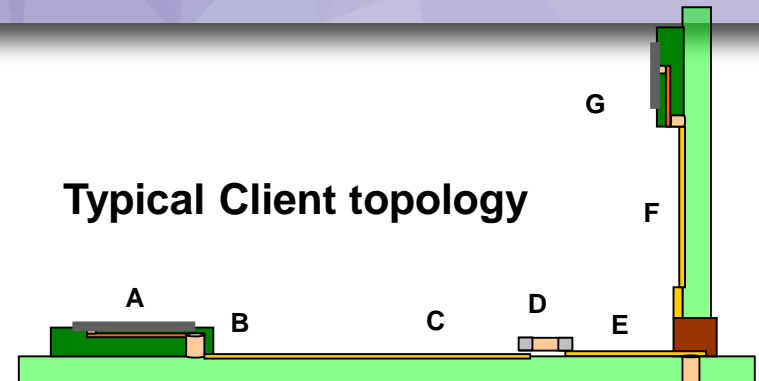
## Client

- Motherboard and adapter
- 1 PCIe connector
- No vias other than connector
- Routed as mstrip
- Channel length: ~10-14"

## Server

- Motherboard, riser card, and adapter
- 2 PCIe connectors
- Several vias on motherboard
- Routed primarily as stripline
- Channel length: ~20"
- Requires Retimer for 16GT/s

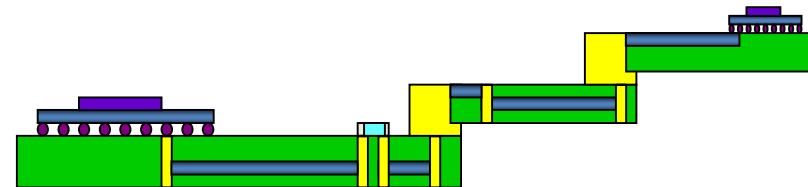
## Channel analysis includes corner cases



Typical Client topology

Seg	Description
A	MCH PKG (transmitter)
B	Break Out
C	MB Main 7"
D	MB post cap
E	Add in card main 3"
F	Add in card PKG Break out
G	Add in card PKG (receiver)

2 Connector Server topology



**PCIe 4.0 targets support for the same channels and lengths as PCIe 3.0**

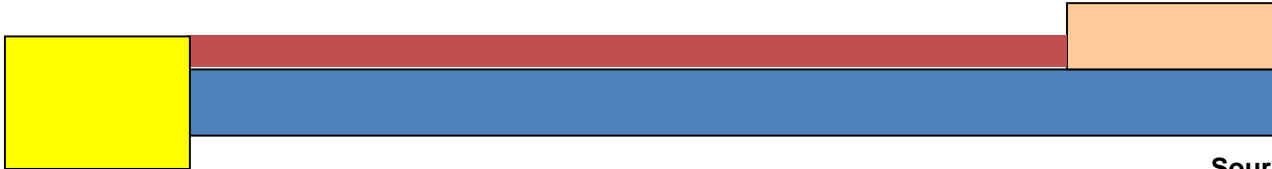
**Longest 2 connector channels will require Retimer**

# CEM MB Tx Test Fixture Topology

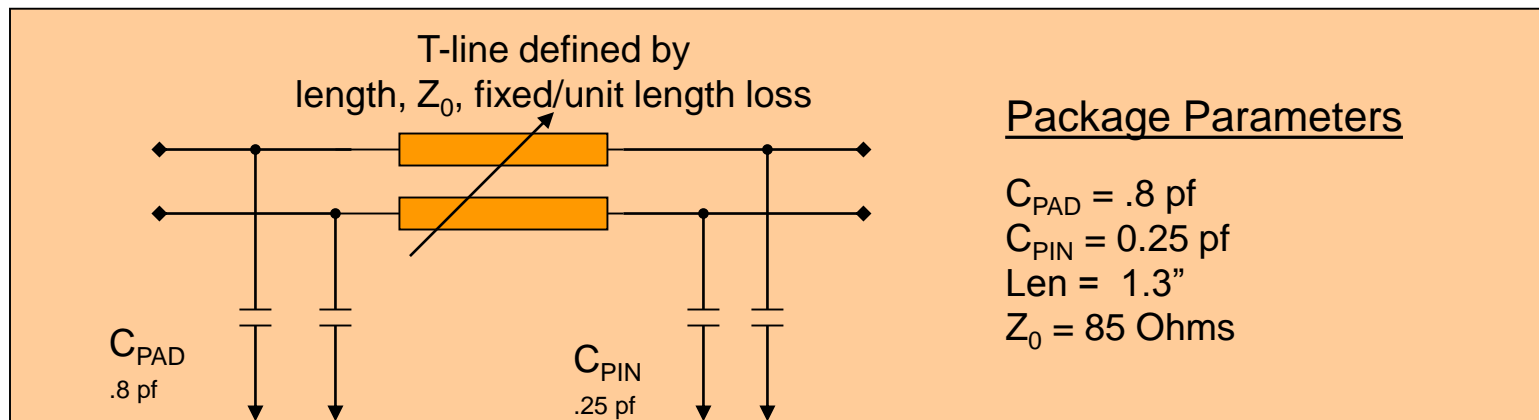


- 4" test fixture

Base Spec RX Package Structure



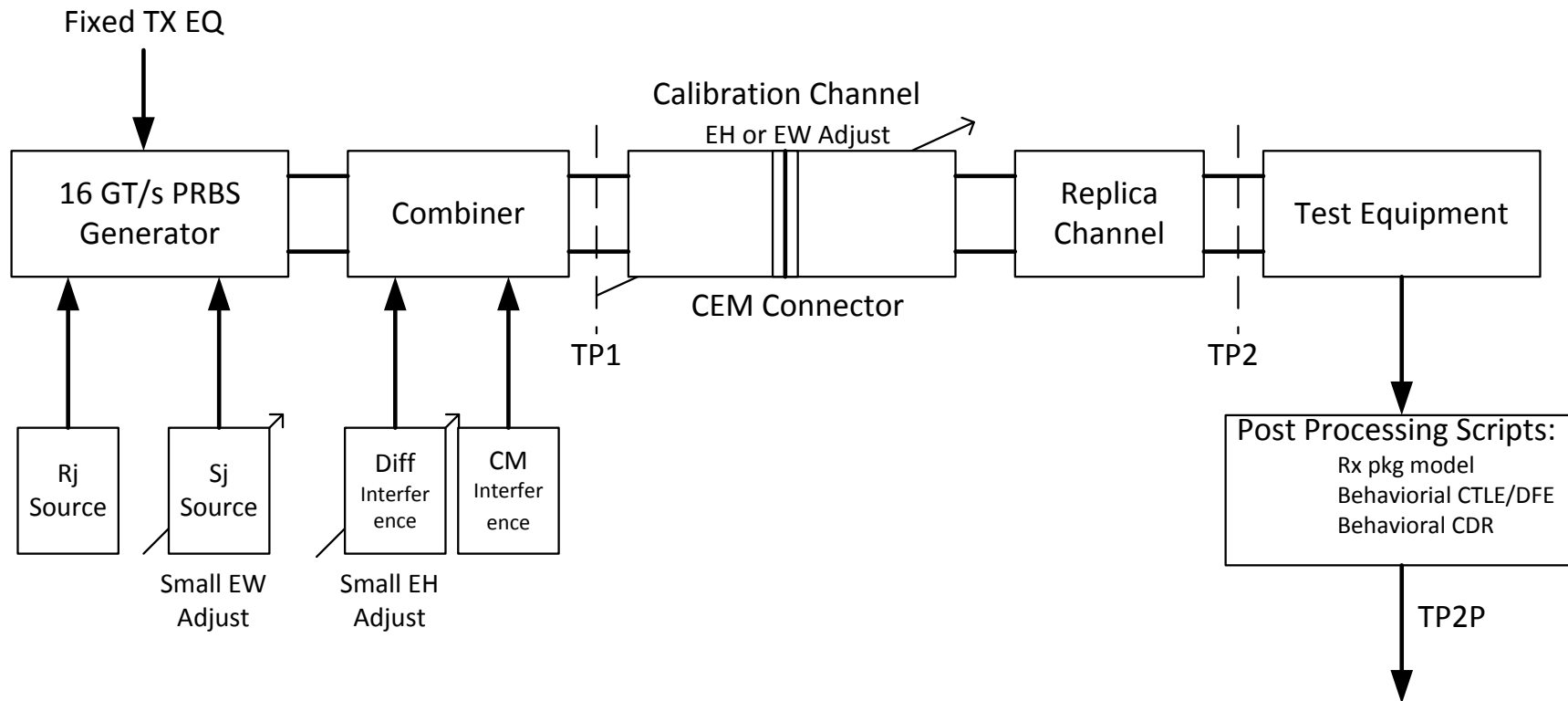
Source: Intel Corporation



- CEM spec pathfinding work showed better correlation with worst case E2E results with fixture with package model on test fixture
- Parameters shown for current CEM 3.0 CLB
- 4.0 CLB Potential Changes
  - Package model will change to  $\sim .3/.4 \text{ pf}$  Cpad
  - Trace length could be reduced from 4"



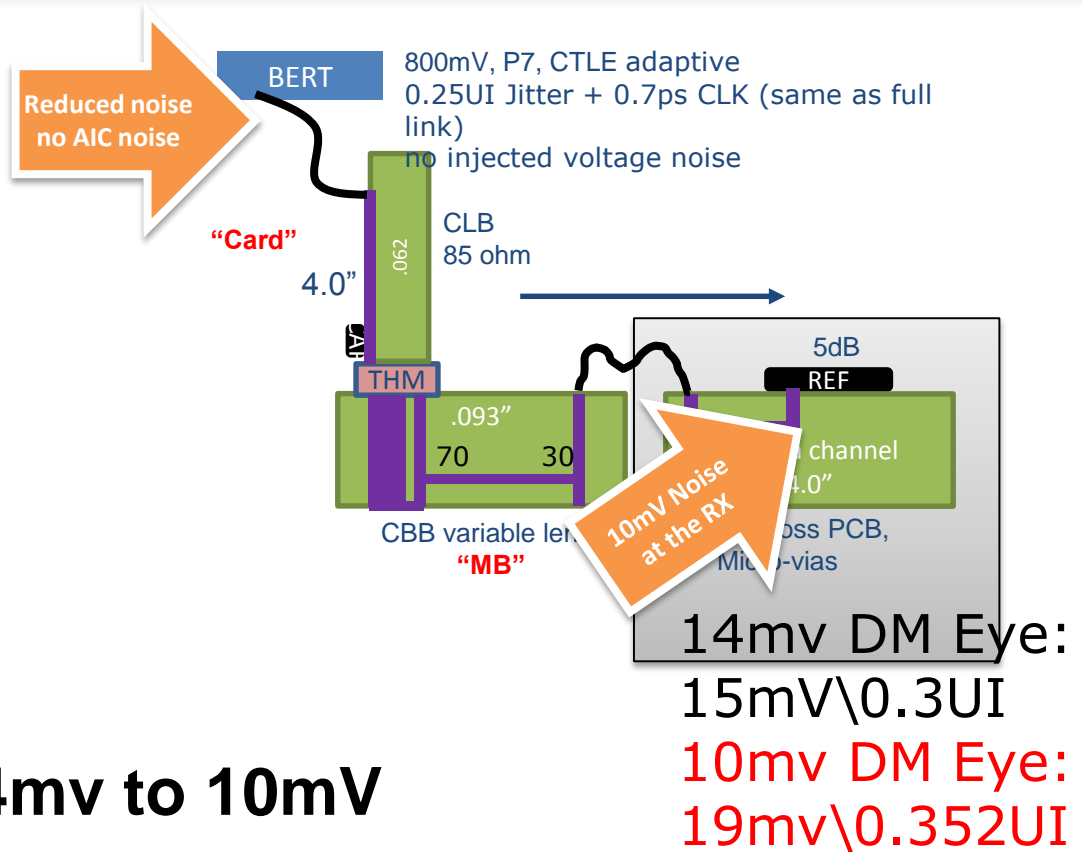
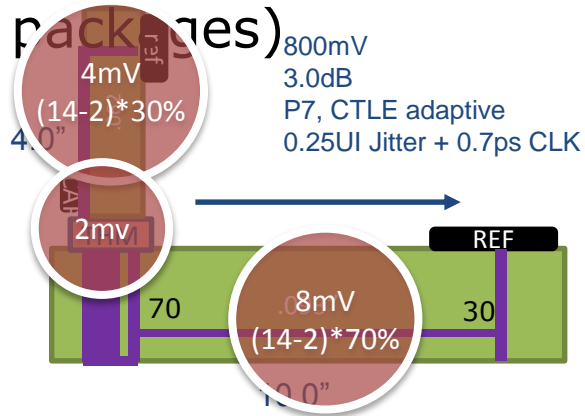
# Calibrating Stressed Eye: Base Spec Direction



15 mV / .3 UI at E-12 BER

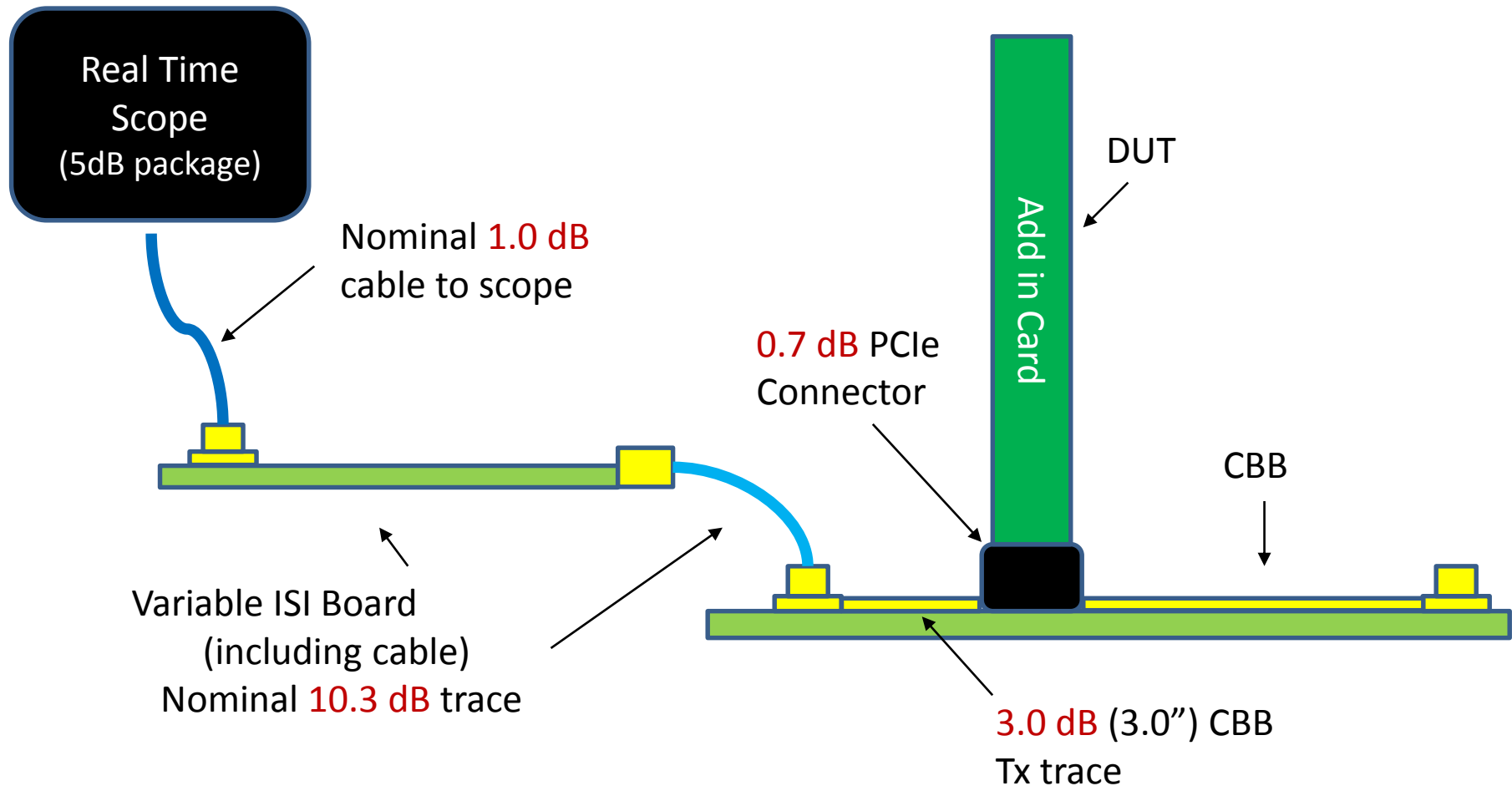
# CEM 4.0 Tx Limits – System Tx Example

Real channel  
(shown reference packages)

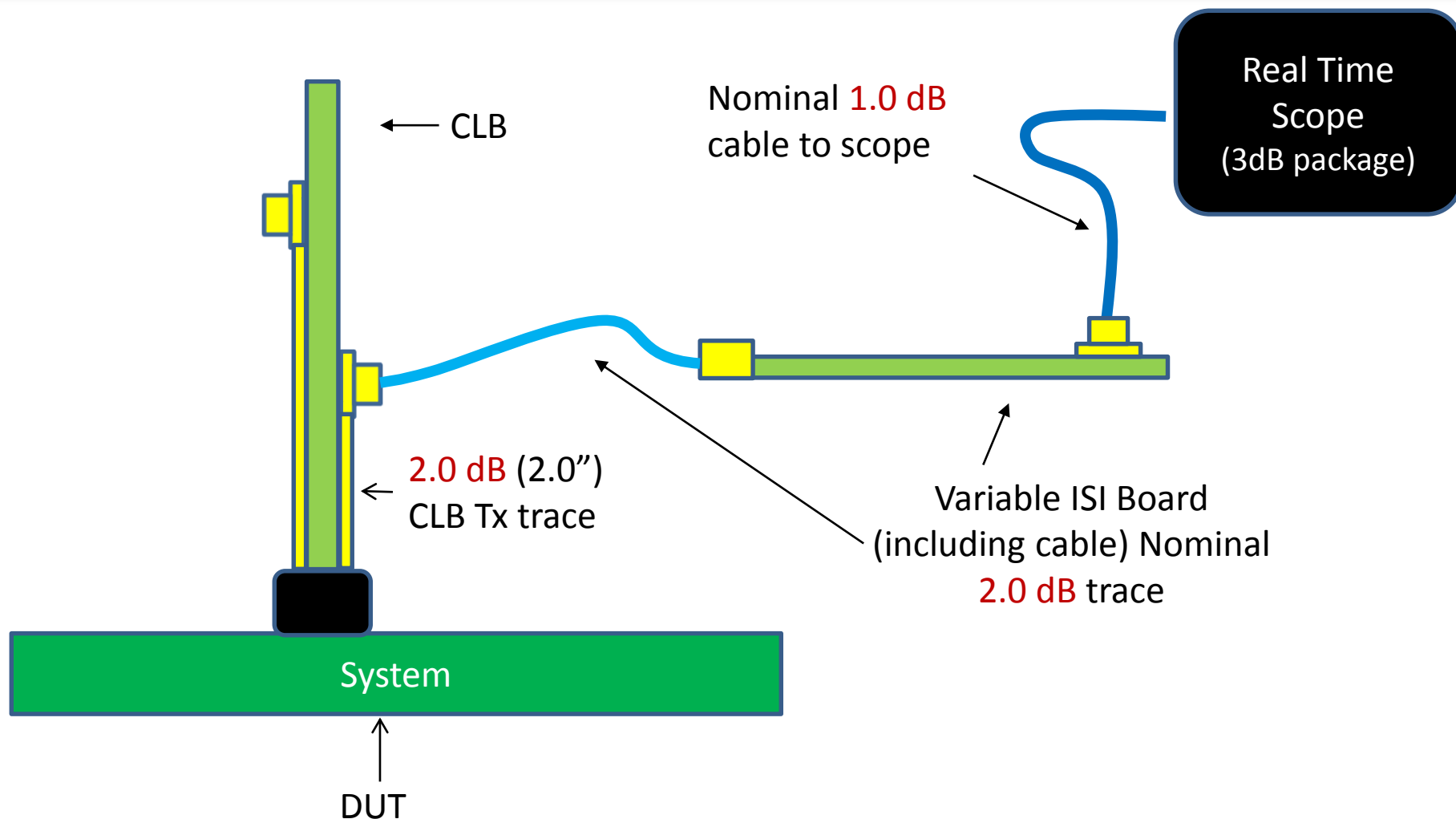


- Reduce noise from 14mV to 10mV
- Simulate to find System TX 4.0 CEM Eye
- This gives the System TX CEM Eye using a simplified approach

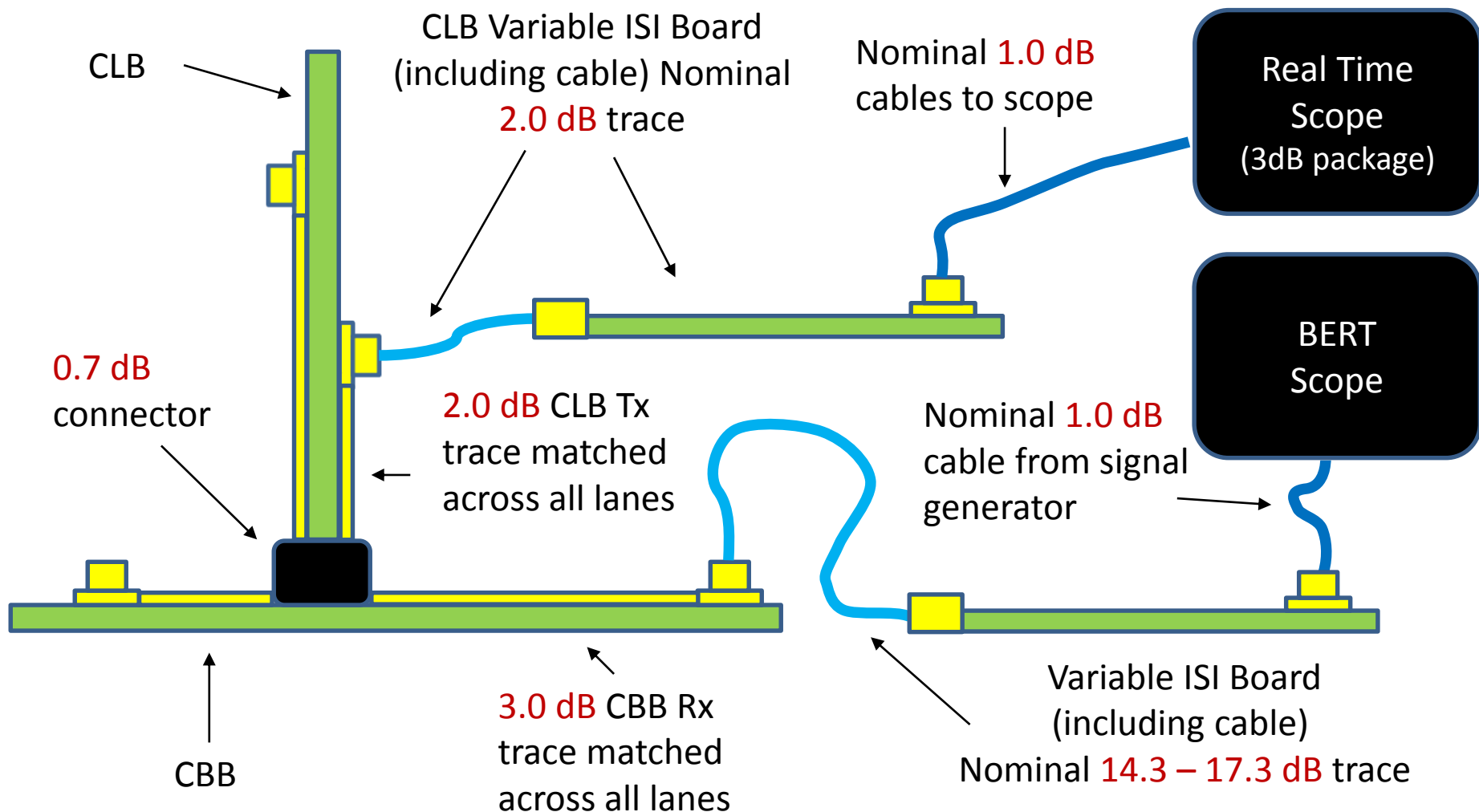
# PCIe 4.0 (Add-in Card) Tx Signal Quality Test at 16 GT/s



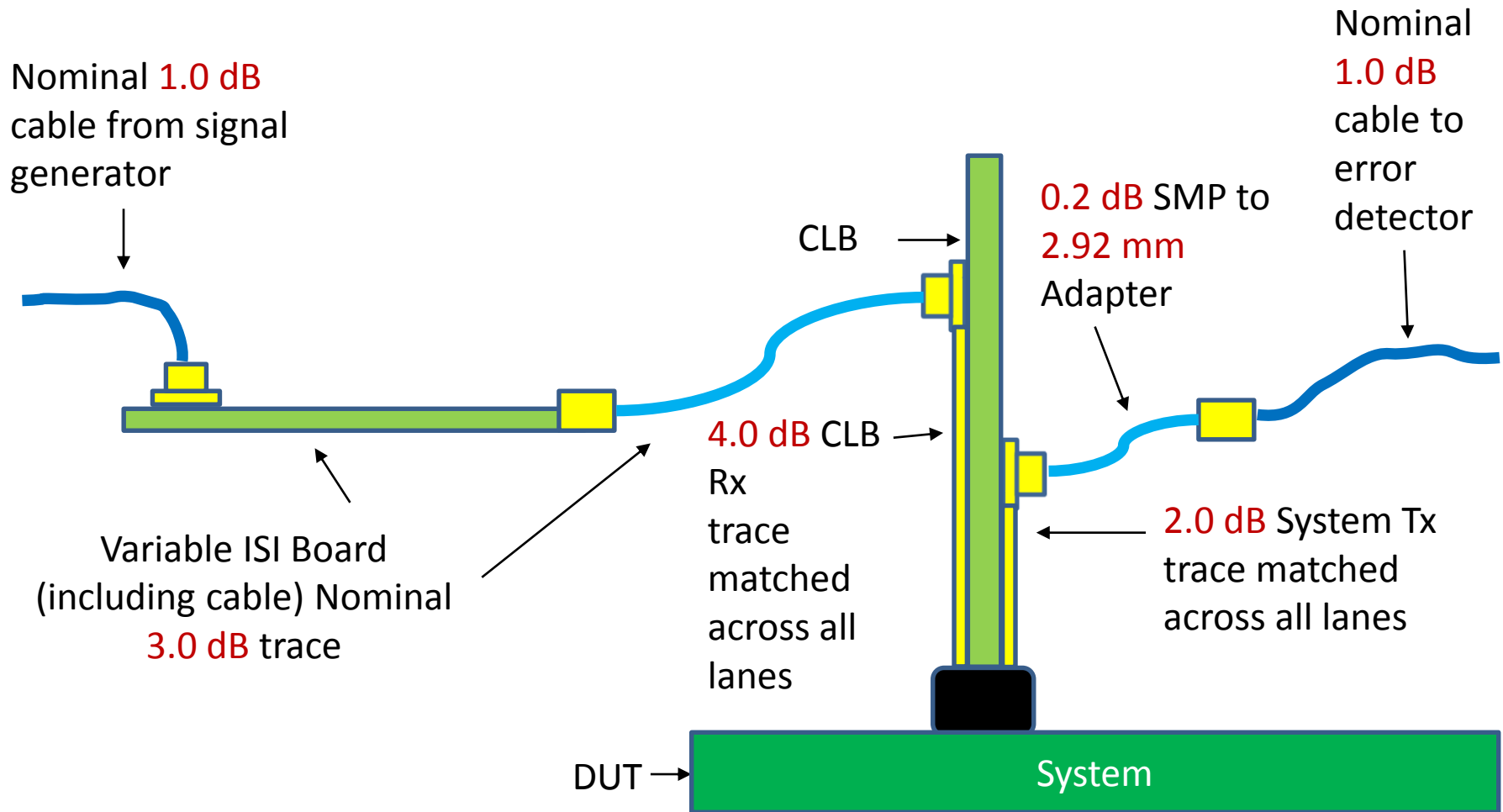
# PCIe 4.0 (System) Tx Signal Quality Test at 16 GT/s



# PCIe 4.0 (Add-in Card) Rx Stressed Eye Calibration at 16GT/s



# PCIe 4.0 (System) Rx Stressed Eye Test at 16GT/s



*In the PCI Express Card Electromechanical Specification, change Table 6-1 in Section 6.1 Connector Pinout, page 87 as follows:*

19	PETp1	Transmitter differential pair, Lane 1	RSVD	
20	PETn1		GND	Ground
21	GND	Ground	PERp1	Receiver differential pair, Lane 1
22	GND	Ground	PERn1	
23	PETp2	Transmitter differential pair, Lane 2	GND	Ground
24	PETn2		GND	Ground
25	GND	Ground	PERp2	Receiver differential pair, Lane 2
26	GND	Ground	PERn2	
27	PETp3	Transmitter differential pair, Lane 3	GND	Ground
28	PETn3		GND	Ground
29	GND	Ground	PERp3	Receiver differential pair, Lane 3
30	<a href="#">PWRBRK</a>	<a href="#">Emergency Power Reduction</a>	PERn3	
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
<b>End of the x4 connector</b>				

# Summary and Conclusions



- **CEM Connector must improve for PCIe 4.0 at 16GT/s**
  - Add-in card PCB enablers for existing PTH connector
  - SMT connectors
- **Direction to support existing PTH connectors with add-in card improvements and SMT connectors pending connector test board data**
- **Same channel reach as for PCIe 3.0**
  - Client: 14 inch, one connector
  - Server: 20 inch, two connectors – with a Retimer
- **Direction to make CEM reference channel same as Base RX stressed eye channel for 4.0**
  - CEM RX call channel/limits match Base RX without need for CEM simulation process
- **For latest PCIe 4.0 specifications, visit [www.pcisig.com](http://www.pcisig.com)**
  - 0.5 CEM 4.0
  - PWRBRK ECR



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